**November 23th Senior Project Meeting**

**Armstrong Hall 187: 12:30-1:30**

**Members in Attendance:** All Members

**Dr. Hernandez Notes for Final Presentation:**

* **Overall:** 
  + Show the top-level chip design and highlight your block in red
  + Focus on System Design, not so much on Implementation
  + Remove ***ALL*** tables explaining signals of each block
  + Discuss flow of data
  + Discuss design choices
* **Cover Slide:**
  + Take out “Complete” from project title
* **Slide 3: - zach**
  + You need performance analysis
  + Why are we using 100Mhz
  + Show control and data flow
* **Slide 5: - zach**
  + Present FPGA as good practice for real-time fabrication
* **Slide 8: - kevin**
  + Discuss data flow and system level design, not implementation
  + Why have a delay of 3 clock cycles?
  + How did you choose the length of the Synch. Chain
  + What is FIFO? Why do you need a FIFO? How long is the FIFO? Why is it that long.
  + Discuss metastability for Synchronizer block
    - What it is?
    - Why is it important?
* **Slide 10: - kevin**
  + Don’t spend too much time discussing the simulations. Explain everything in diagram model, and the simulation just is to show that it works, it delays, then go on
  + *\*Testbench is just proof of the system level design you already explained*
* **Slide 14: - kevin**
  + Explain BIST? Why is it there?
  + Show it generates sawtooth wave
  + Functionality explained before and testbench once again just verify what you are saying worked
* **Slide 20: - dhruvit**
  + Separation of signals: FM Band 🡪 radio signal you want to listen to
  + Restoration of Signals 🡪 get rid of noise
* **Slide 21: - dhruvit**
  + How characteristic of filter creates transfer function
  + The inverse FFT of the filter response in frequency domain 🡪yield convolution (difference equation🡪discrete type)
* **Slide 22: - dhruvit**
  + Explain data flow
  + Explain how state machine supply correct coeff.
  + Show how/why the difference equation is implemented
  + Explain why we saturate at the end (not throughout)/ why no monitoring until end
  + Accumulator value is set to \_\_\_?
  + Why this is a good design?
* **Slide 24: - dhruvit**
  + Delete
* **Slide 26: - julie**
  + Explain use of sticky bits
  + Give an update but educate audience
* **Slide 29: - julie**
  + Delete. Discuss in slide 27
* **Slide 32: - julie**
  + Delete. Just discuss this in previous slides
* **Slide 34: - whitely**
  + Change 1024 to 512 & associated transfer time
  + Explain protocol
  + What drives clock
  + Discuss starting bit
* **Slide 35: - whitely**
  + Make connection between why you need state machine and slide before
* **Slide 36: - whitely**
  + Do not say signal names. Just explain flow of data.
* **Slide 39: - zach**
  + Emphasize positive
  + EDA tools🡪 complex tools/ going through the motion
  + Discuss how TCNJ has never done a project with chip design using these tools